EE/CprE/SE 491 WEEKLY REPORT 7

Date: ***Mar 21st, 2023 – Apr 2nd, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

For this two-week span, we further honed in on how we are going to approach the final design. Some team members continued to design analog circuits through the open-source workflow. We currently have created a simulated a 1-bit DAC and a 1-bit ADC. We also worked on creating layouts in Magic and passing LVS tests. After hours of troubleshooting, we were able to properly extract the correct netlist from Xschem and compare it against an extracted netlist from Magic to pass LVS on the 1-bit DAC. At the end of this two-week period, we began work on the transimpedance amplifier, plus the sample and hold circuitry.

Past week accomplishments

- Joshua Thater
    - Created a new layout for 1-bit DAC so that it would have a proper netlist
    - Passed LVS test between schematic and layout of 1-bit DAC
    - Began work on 1t1r cell and transimpedance amplifier
- Aiden Petersen
    - Created behavioral model of reram crossbar
        - Got simulation results
        - Can do MAC
- Matt Ottersen

    - Was able to get the 1 bit ADC to simulate properly
    - Was able to create and simulate a sample and hold circuit
- Regassa Dukele
    - Created a schematic of a 3-bit ADC
    - Working on verifying by simulation

Pending issues

- How to simulate the ReRAM cell (Looks like we might have to convert spice netlist to Verilog A and run simulation using Xyce?)
- How to properly create a layout of ReRAM cell using Magic

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Found out how to get designs to pass LVS tests. Got a 1-bit DAC to pass LVS & began work on other circuitry.	5	45
Aiden Petersen	Created behavioral model emulating reram crossbar	8	33
Matt Ottersen	Finished the 1 bit ADC and designed sample and hold	7	38
Regassa Dukele	I'm currently in the process of creating a schematic of a 3-bit ADC	6	37.5

Plans for the upcoming week

- Joshua Thater
    - Create transimpedance amplifier schematic and simulate it
    - Create a layout for the transimpedance amplifier
    - Attempt to get a simulation of 1t1r cell
- Aiden Petersen
    - Further refine behavioral model
- Matt Ottersen
    - Create the Layouts for ADC and sample and hold and get them to pass LVS
- Regassa Dukele
    - Creating a fully functional schematic for a 3-bit ADC with the result.
    - The reason: it will significantly improve performance/ no need for quantization over a one-bit ADC.